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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/804,237

03/19/2004

Yonghua Song

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EXAMINER

TRA, ANH QUAN

ART UNIT

PAPER NUMBER

2816

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
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3 MONTHS

01/09/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

**Office Action Summary**

Application No.

10/804,237

Applicant(s)

SONG, YONGHUA

Examiner

Quan Tra

Art Unit

2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 29 November 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-72 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-21 and 41-44 is/are allowed.
- 6) ☒ Claim(s) 22-25, 29, 31-34 and 45-72 is/are rejected.
- 7) ☒ Claim(s) 26-28, 30 and 35-40 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### DETAILED ACTION

This office action is in response to the amendment filed 11/29/06. The some of the rejections in previous office action are maintained.

#### ***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 22, 23, 25, 29, 32 and 34 are rejected under 35 U.S.C. 102(b) as being anticipated by Nagaraj et al. (USP 5642077).

As to claim 22, Nagaraj's figure 1 shows a temperature and process independent analog integrated circuit comprising: analog integrated function means (122, 120, 140, 104) for providing first and second output signals responsive to a first differential input signal and a second differential input; first loading means (124) for providing an output voltage in response to the first output signal, a common mode voltage signal (VCM), and a compensation control signal (at the gate); second loading means (138) for providing an output voltage in response to the second output signal, the common mode voltage signal, and the compensation control signal; and compensation circuit (142, 150) for generating the compensation control signal to compensate for changes due to temperature and manufacturing variations.

As to claim 23, figure 1 shows that the analog integrated function means is selected from the group consisting of multipliers, adaptive filters, function generators, modulators, and neural networks.

As to claim 25, figure 1 shows that the first and second loading means comprise MOS transistors.

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As to claim 29, figure 1 shows that biasing means to provide the common mode voltage to the first and second loading means (inherent).

Claims 32 and 34 recite similar limitations of claims above. Therefore, they are rejected for the same reasons.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 24 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's prior art figure 3 in view of Nagaraj et al. (USP 5642077).

Applicant's prior art figure 3 shows all limitations of the claim except for the load in communication with a common mode voltage and a compensation circuit. However, Nagaraj's figure 1 shows a circuit having load (124, 138) in communication with compensation circuit (142, 150) and common mode voltage VCM in order to reduce noise. Therefore, it would have been obvious to one having ordinary skill in the art to use Nagaraj's load and compensation circuits for Applicant's prior art's load for the purpose of reducing noise.

5. Claim 31 and 45-72 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagaraj et al. (USP 5642077).

As to claim 31, Nagaraj's figure 1 fails to teach that the common mode voltage is substantially proportional to a semiconductor bandgap voltage. However, it is notoriously well known in the art that bandgap voltage is temperature independent. Therefore, it would have

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been obvious to one having ordinary skill in the art to use bandgap voltage to generate the common mode voltage VCM for the purpose providing temperature independent voltage.

As to claim 45, the modified Nagaraj's figure 1 shows an integrated circuits comprising: an analog function circuit (120, 116, 140, 104); a differential loading device (130, 132) in communication with a differential output of the analog function circuit; a compensation circuit (142, 150) in communication with the differential loading device; and a biasing circuit (circuit, not shown, that generates VCM, VDD or bias voltage to the current source 142) in communication with a common mode node of the differential loading device and an input of the compensation circuit, wherein the biasing circuit provides a common mode voltage to the common mode node of the differential loading device and the compensation circuit, and wherein the common mode voltage is independent of temperature and manufacturing process variations (see the rejection of claim 31).

As to claim 46, figure 1 shows that the biasing circuit provides a plurality of control bias voltage signals (VCM, Vdd) to the compensation circuit.

As to claim 47, figure 1 shows that the compensation circuit provides a bias voltage to the differential loading device, and wherein the bias voltage is independent of temperature and manufacturing process variations.

As to claim 48, figure 1 shows that the bias voltage varies a differential loading of the differential loading device.

As to claim 49, figure 1 shows that the bias voltage is comprised of at least the common mode voltage and the plurality of control bias voltage signals (Vdd and bias voltage of the current source 142, figure 3 shows example of current source).

As to claim 50, figure 1 shows that the bias voltage controls a loading on at least one voltage signal associated with the differential loading device.

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As to claim 51, figure 1 shows that the differential loading device provides the temperature and process independent output voltage comprised of at least a differential output signal of the analog function circuit, the common mode voltage and the bias voltage.

As to claim 52, figure 1 shows that the plurality of control bias voltage signals are substantially proportional to a semiconductor bandgap voltage (see the rejection of claim 31).

As to claim 53, figure 1 shows that the common mode voltage is substantially proportional to a semiconductor bandgap voltage (see the rejection of claim 31).

As to claim 54, figure 1 shows that the analog function circuit comprises a circuit selected from the group consisting of multipliers, adaptive filters, modulators and neural networks.

As to claim 55, figure 1 shows that the differential loading device comprises first and second transistors (124, 138), wherein the first transistor comprises a first terminal responsive to a first output terminal of the analog function circuit, a second terminal in communication with the common mode node, and a first control terminal; wherein the second transistor comprises a third terminal responsive to a second output terminal of the analog function circuits a fourth terminal in communication with the common mode node, and a second control terminals and wherein the biasing circuit is in communication with the first and second control terminals.

Claims 56-72 recite similar limitations of claims above. Therefore, they are rejected for the same reasons.

***Allowable Subject Matter***

6. Claims 1-21 and 41-44 are allowed.

7. Claims 26-28, 30 and 35-40 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

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Claims 1-21 and 41-44 are and claims 26-28, 30 and 35-40 would be allowable because the prior art fails to teach or suggest that the compensation circuit comprising the third MOS transistor and differential amplifier connected as disclosed.

### ***Response to Arguments***

8. Applicant's arguments filed been fully considered but they are not persuasive.

Applicant argues that Nagaraj fails to show a first and second differential input signals. The Examiner respectfully disagrees. Nagaraj's signals  $V_{in+}$  and  $V_{in-}$  form a pair of differential input signals. With broadest reasonable interpretation,  $V_{in+}$  is one differential input signal of pair differential input signals, and  $V_{in}$  is another differential input signal of the pair.

Applicant further argues that Nagaraj circuit does not generate a compensation control signal to compensate for changes due to temperature and manufacturing variations. The Examiner respectfully disagrees. It is inherent that Nagaraj's output 150 is varied as temperature varies, and the outputs of 124 and 138 are varied as the output 150 varies. Therefore, the output 150 generates a compensation control signal to compensate for changes due to temperature and manufacturing variations.

Applicant further argues that there is no motivation to add a band gap circuit to Nagaraj's. However, it is well known that band gap voltage is a voltage that is independent of temperature and process of variation. The output voltage will be more precise if temperature independent voltage is used. One skilled in the art would have motivated to use band gap circuit to provide supply voltage  $V_{dd}$  or VCM voltage for the purpose of obtaining precision output voltages.

### ***Conclusion***

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

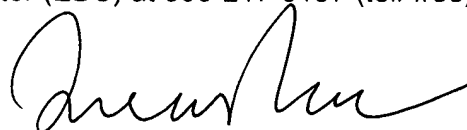
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A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



QUAN TRA  
PRIMARY EXAMINER  
ART UNIT 2816

January 4, 2007